DAQ

NI 671*X*/673*X*
User Manual

Analog Voltage Output Devices
for PCI/PXI/CompactPCI/PCMCIA Bus Computers

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Worldwide Technical Support and Product Information

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The NI 6711/6713/6733 for PCI/PXI/CompactPCI, the NI 6731 for PCI, and the NI 6715 for PCMCIA are warranted against defects in materials and workmanship for a period of one year from the date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

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Compliance

FCC/Canada Radio Frequency Interference Compliance*

Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.

Consult the FCC Web site `fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity**, may cause interference to radio and television reception. Classification requirements are the same for the FCC and the Canadian DOC.

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

Readers in the European Union (EU) must refer to the Manufacturer's Declaration of Conformity (DoC) for information** pertaining to the CE Mark compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of the following National Instruments devices and contains information concerning their operation and programming:

- NI 6711 for PCI/PXI/CompactPCI
- NI 6713 for PCI/PXI/CompactPCI
- NI 6715 for PCMCIA (the DAQCard-6715)
- NI 6731 for PCI
- NI 6733 for PCI/PXI/CompactPCI

These NI devices are multifunction analog output (AO), digital I/O (DIO), and timing I/O (TIO) devices and have the following features:

- PCI/PXI-6711 has four 12-bit AO channels, two counters, and eight DIO channels.
- PCI/PXI-6713 has eight 12-bit AO channels, two counters, and eight DIO channels.
- PCI-6731 has four 16-bit AO channels, two counters, and eight DIO channels.
- PCI/PXI-6733 has eight 16-bit AO channels, two counters, and eight DIO channels.
- DAQCard-6715 for PCMCIA has eight 12-bit AO channels, two counters, and eight DIO channels.

Conventions Used in This Manual

The following conventions are used in this manual.

<> Angle brackets enclose the name of a key on the keyboard (for example, <option>). Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name (for example, DIO<3..0>).

♦ The ♦ indicates that the text following it applies to only to a specific device.

This icon denotes a note, which alerts you to important information.

This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on

	the product, see the *Safety Information* section in Chapter 1, *Introduction*, for precautions to take.
bold	Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept. This font also denotes text from which you supply the appropriate word or value, as in NI-DAQ 6.*X*.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI 671*X*	NI 671*X* refers to the PCI/PXI-6711/6713 and the DAQCard-6715 unless otherwise noted.
NI 673*X*	NI 673*X* refers to the PCI-6731 and the PCI/PXI-6733 unless otherwise noted.
Platform	Text in this font denotes a specific platform and indicates that the text following it applies only to that platform.

National Instruments Documentation

The NI 671X/673X User Manual is one piece of the documentation set for the DAQ system. You could have other types of documentation, depending on the hardware and software in the system. Use the documentation you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, read this manual first. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- SCXI hardware user manuals—If you are using SCXI, read these manuals next for information about signal connections and module configuration. The user manuals explain in greater detail how the modules work, and they also contain application hints.
- DAQ hardware documentation—This documentation has detailed information about the DAQ hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and

configuration instructions, specification information about the DAQ hardware, and application hints.

- Software documentation—You may have both application software and NI-DAQ documentation. After you set up the hardware system, use either the application software documentation or the NI-DAQ documentation to help you write your application. NI application software includes LabVIEW and Measurement Studio. If you have a large, complicated system, you should look through the software documentation before you configure the hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making the connections.
- SCXI chassis manuals—If you are using SCXI, read these manuals for maintenance information on the chassis and installation instructions.

Related Documentation

The following documents contain information you may find helpful:

- *DAQ Quick Start Guide,* available at `ni.com/manuals`
- *DAQ-STC Technical Reference Manual,* available at `ni.com/manuals`
- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals,* available at `ni.com/zone`
- *NI-DAQ User Manual for PC Compatibles*, available at `ni.com/manuals`
- *PCI Local Bus Specification Revision 2.2*
- *PICMG CompactPCI 2.0 R3.0*
- *PXI Specification Revision 2.0*

1

Introduction

This chapter describes the NI 671*X*/673*X*, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack the NI 671*X*/673*X*.

About the NI 671*X*/673*X* Device

The NI 671*X*/673*X* is a Plug and Play, analog output, digital, and timing I/O device for PXI/PCI/CompactPCI or PCMCIA bus computers.

The NI 671*X* features a 12-bit D/A converter (DAC) with update rates up to 1 MS/s/channel for voltage outputs, while the NI 673*X* features a 16-bit DAC per channel with update rates up to 1 MS/s/channel for voltage outputs. In addition, the NI 671*X*/673*X* features eight lines of TTL-compatible DIO, and two 24-bit counter/timers for TIO. The NI 6711/6731 features four voltage output channels, while the NI 6713/6715/6733 features eight voltage output channels.

The NI 671*X*/673*X* device has no DIP switches, jumpers, or potentiometers, so you can easily software configure and calibrate it. This feature is made possible by the NI MXI Interface to Everything (MITE) bus interface chip that connects the device to the PCI I/O bus. The MITE implements the PCI Local Bus Specification so that the interrupts and base memory addresses are software configured.

The NI 671*X*/673*X* device uses the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC has three timing groups that control AI, AO, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and have a maximum timing resolution of 50 ns. The AI section of the DAQ-STC is unused by the NI 671*X*/673*X*.

- NI 6711/6713/673*X* only

  The NI 6711/6713/673*X* device uses the Real-Time System Integration (RTSI) bus to easily synchronize several measurement functions to a common trigger or timing event. The RTSI bus consists of a RTSI bus interface and a ribbon cable to route timing and trigger signals between several functions on as many as five DAQ devices in the computer.

Note If you are using the PXI-6711/6713/6733 in a PXI chassis, RTSI lines, known as the PXI trigger bus, are part of the backplane. Therefore, you do not need the RTSI cable for system triggering and timing on the PXI.

- NI 6715 only

  The NI 6715 provides access to timing and triggering signals through the I/O connector for synchronization to other DAQ devices or timing signals.

  Detailed specifications of the NI 671*X*/673*X* are in Appendix A, *Specifications*.

Using PXI with CompactPCI

- NI 6711/6713/6733 for PXI/CompactPCI only

  Using PXI-compatible products with standard CompactPCI products is an important feature provided by the *PXI Specification Revision 2.0*. If you use a PXI-compatible plug-in device in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you can use the basic plug-in device functions. For example, the PXI trigger bus on the NI 6711/6713/6733 device is available in a PXI chassis but not in a CompactPCI chassis.

  The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The NI 6711/6713/6733 works in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R3.0* specification.

  PXI-specific features, RTSI bus trigger, RTSI Clock, and Serial Communication are implemented on the J2 connector of the CompactPCI bus. Table 1-1 lists the J2 pins used by the NI 6711/6713/6733 for PXI/CompactPCI, which is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. Even if the sub-bus is capable of

driving these lines, the NI 6711/6713/6733 is still compatible as long as those pins on the sub-bus are disabled by default and are never enabled. Damage can result if these lines are driven by the sub-bus.

Table 1-1. NI 6711/6713/6733 for PXI/CompactPCI J2 Pin Assignment

NI 673*X* Signal	PXI Pin Name	PXI J2 Pin Number
RTSI Trigger<0..5>	PXI Trigger<0..5>	B16, A16, A17, A18, B18, C18
RTSI Trigger 6	PXI Star Trigger	D17
RTSI Clock	PXI Trigger (7)	E16
Serial Communication	LBR (6, 7, 8, 9, 10, 11, 12)	EI5, A3, C3, D3, E3, A2, B2

What You Need to Get Started

To set up and use the NI 671*X*/673*X*, you need the following:

- ❑ A computer
- ❑ One of the following devices:
  - NI 6711 for PCI/PXI/CompactPCI
  - NI 6713 for PCI/PXI/CompactPCI
  - NI 6715 for PCMCIA (the DAQCard-6715)
  - NI 6731 for PCI
  - NI 6733 for PCI/PXI/CompactPCI
- ❑ *NI 671X/673X User Manual*
- ❑ One of the following versions of NI-DAQ, available at `ni.com/download`:
  - NI 6711/6713—NI-DAQ for Mac OS version 6.6 or later, or NI-DAQ for PC Compatibles version 6.5 or later
  - NI 6715—NI-DAQ for PC Compatibles version 6.7 or later
  - NI 673*X*—NI-DAQ for PC Compatibles version 6.9.2 or later

- ❑ One of the following:
  - LabVIEW **(Mac OS[1] or Windows)**
  - Measurement Studio **(Windows)**
  - Conventional programming environment
- ❑ SH68-68-EP cable (for NI 6711/6713/673*X*)
- ❑ SHC68-68-EP or SHC68U-68-EP cable (for NI 6715)
- ❑ One of the following:
  - BNC 2110 signal connector block
  - SCB-68 shielded terminal block
  - CB-68LP terminal block

Unpacking

The NI 671*X*/673*X* is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge (ESD) can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the computer.

Store the NI 671*X*/673*X* in the antistatic envelope when not in use.

[1] NI 6711/6713 only

Software Programming Choices

When programming the National Instruments DAQ hardware, you can use NI application development environment (ADE) software or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which ships with the NI 671*X*/673*X*, has an extensive library of functions that you can call from the ADE. These functions allow you to use all the features of the NI 671*X*/673*X*.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to the code. Whether you use LabVIEW, Measurement Studio, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

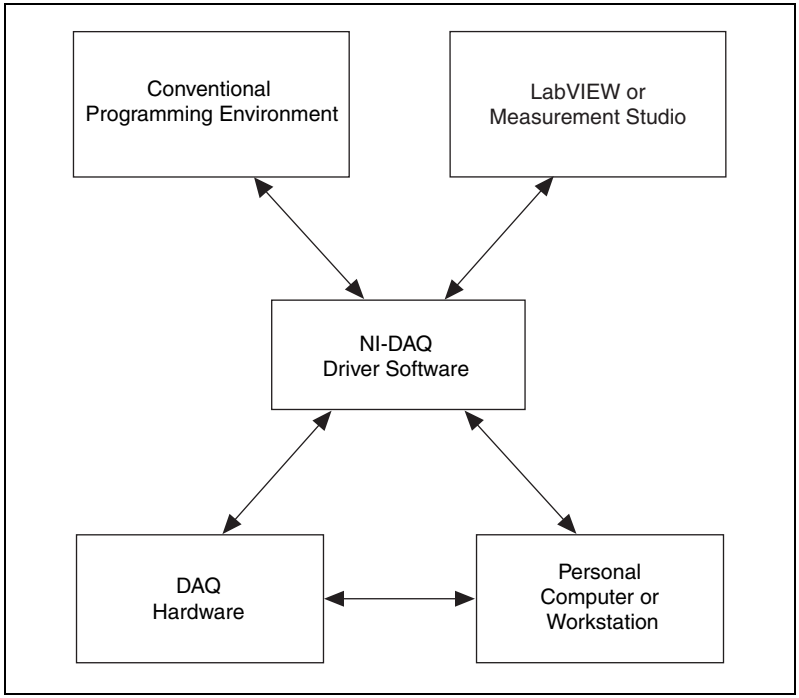


Figure 1-1. The Relationship Between the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at ni.com.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows/CVI, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design the test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries, ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

Using LabVIEW or Measurement Studio greatly reduces the development time for your data acquisition and control application.

Optional Equipment

NI offers a variety of products to use with the NI 671*X*/673*X*, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies
- Connector blocks, and shielded and unshielded 50- and 68-pin screw terminals
- RTSI bus cables
- Low channel-count digital signal conditioning modules, devices, and accessories

For more specific information about these products, call the office nearest you or refer to the NI catalog at ni.com/catalog.

Custom Cabling

NI offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

The following guidelines can be useful if you want to develop your own cable:

- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI.

The following list gives recommended connectors that mate to the I/O connector on the NI 6711/6713/673*X*:

- Honda 68-position, solder cup, female connector
- Honda backshell

The following list gives recommended connectors that mate to the I/O connector on the NI 6715:

- Amp 68-position, VHDCI
- Amp backshell

Safety Information

The following section contains important safety information that you *must* follow when installing and using the NI 671*X*/673*X*.

Do *not* operate the NI 671*X*/673*X* in a manner not specified in this document. Misuse of the device can result in a hazard. You can compromise the safety protection built into the NI 671*X*/673*X* if the device is damaged in any way. If the NI 671*X*/673*X* is damaged, return it to NI for repair.

Do *not* substitute parts or modify the NI 671*X*/673*X* except as described in this document. Use the device only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the NI 671*X*/673*X*.

Do *not* operate the NI 671*X*/673*X* in an explosive atmosphere or where there may be flammable gases or fumes. Operate the device only at or

below the pollution degree stated in Appendix A, *Specifications*. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

Clean the NI 671*X*/673*X* with a soft nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

You *must* insulate signal connections for the maximum voltage for which the NI 671*X*/673*X* is rated. Do *not* exceed the maximum ratings for the device. Remove power from signal lines before connecting them to or disconnecting them from the NI 671*X*/673*X*.

Operate the NI 671*X*/673*X* only at or below the installation category stated in Appendix A, *Specifications*.

The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to MAINS[1]. This category is a signal level such as voltages on a printed wire board (PWB) on the secondary of an isolation transformer.

  Examples of Installation Category I are measurements on circuits not derived from MAINS and specially protected (internal) MAINS-derived circuits.

- Installation Category II is for measurements performed on circuits directly connected to the low-voltage installation. This category refers to local-level distribution such as that provided by a standard wall outlet.

  Examples of Installation Category II are measurements on household appliances, portable tools, and similar equipment.

[1] MAINS is defined as the electricity supply system to which the equipment concerned is designed to be connected either for powering the equipment or for measurement purposes.

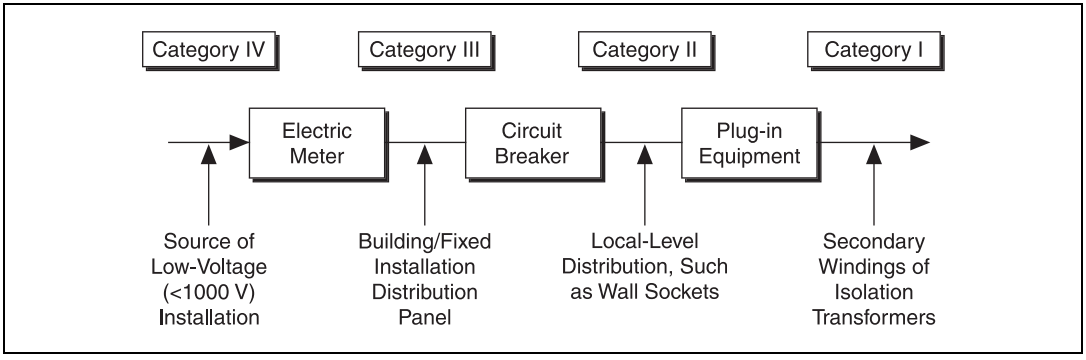
- Installation Category III is for measurements performed in the building installation. This category is a distribution level referring to hardwired equipment that does not rely on standard building insulation.

  Examples of Installation Category III include measurements on distribution circuits and circuit breakers. Other examples of Installation Category III are wiring including cables, bus-bars, junction boxes, switches, socket outlets in the building/fixed installation, and equipment for industrial use, such as stationary motors with a permanent connection to the building/fixed installation.

- Installation Category IV is for measurements performed at the source of the low-voltage (<1,000 V) installation.

  Examples of Installation Category IV are electric meters, and measurements on primary overcurrent protection devices and ripple-control units.

Below is a diagram of a sample installation.



2

Installing and Configuring the NI 671*X*/673*X*

This chapter explains how to install and configure the NI 671*X*/673*X*.

Installing the Software

Complete the following steps to install the software before you install the NI 671*X*/673*X*.

1. Install the ADE, such as LabVIEW or Measurement Studio, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* included with the device.

Note It is important to install NI-DAQ before installing the NI 671*X*/673*X* to ensure that the device is properly detected.

Installing the Hardware

You can install the NI 6711/6713/673*X* in any available PCI system slot or 5 V PXI expansion slot in the computer. You can install the DAQCard-6715 in any available CardBus-compatible Type II PCMCIA 5 V PC Card slot in the computer. However, to achieve best noise performance, leave as much room as possible between the NI 671*X*/673*X* and other devices and hardware.

The following are general installation instructions, so consult the computer user manual or technical reference manual for specific instructions and warnings.

Note Follow the guidelines in the computer documentation for installing plug-in hardware.

- PCI-6711/6713/673*X*
  1. Power off and unplug the computer.
  2. Remove the top cover of the computer.

3. Make sure there are no lighted LEDs on the motherboard. If any are lit, wait until they go out before continuing the installation.
4. Remove the expansion slot cover on the back panel of the computer.
5. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section in Chapter 1, *Introduction*.
6. Insert the PCI-6711/6713/673*X* into a PCI system slot. Gently rock the device to ease it into place. It can be a tight fit, but do *not* force the device into place.
7. If required, screw the mounting bracket of the PCI-6711/6713/673*X* device to the back panel rail of the computer.
8. Visually verify the installation. Make sure the device is not touching other devices or components and is fully inserted into the slot.
9. Replace the cover.
10. Plug in and power on the computer.

The PCI-6711/6713/673*X* is now installed.

- PXI-6711/6713/6733

You can install the PXI-6711/6713/6733 in any available PXI slot in the PXI or CompactPCI chassis.

Note The PXI-6711/6713/6733 has connections to several reserved lines on the CompactPCI J2 connector. Before installing the PXI-6711/6713/6733 in a CompactPCI system that uses J2 connector lines for a purpose other than PXI, see the *Using PXI with CompactPCI* section in Chapter 1, *Introduction*.

1. Power off and unplug the PXI or CompactPCI chassis.
2. Choose an unused PXI or CompactPCI peripheral slot.

Note For maximum performance, install the PXI-6711/6713/6733 in a slot that supports bus arbitration or bus master cards. The PXI-6711/6713/6733 contains onboard bus master DMA logic that can operate only in such a slot. If you choose a slot that does not support bus masters, you will have to disable the onboard DMA controller using the software. PXI-compliant chassis must have bus arbitration for all slots.

3. Make sure there are no lighted LEDs on the chassis. If any are lit, wait until they go out before continuing the installation.
4. Remove the filter panel for the peripheral slot that you have chosen.

5. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section in Chapter 1, *Introduction*.
6. Insert the PXI-6711/6713/6733 device in the 5 V slot. Use the injector/ejector handle to fully inject the device into place.
7. Screw the front panel of the PXI-6711/6713/6733 to the front panel mounting rails of the PXI or CompactPCI chassis.
8. Visually verify the installation. Make sure the device is not touching other devices or components and is fully inserted into the slot.
9. Plug in and power on the PXI or CompactPCI chassis.

The PXI-6711/6713/6733 is now installed.

- DAQCard-6715

You can install the DAQCard-6715 for PCMCIA in any available CardBus-compatible Type II PCMCIA slot. Consult the computer manufacturer for information about slot compatibility.

1. Power off the computer. If the computer and operating system support hot insertion, you may insert or remove the DAQCard-6715 at any time, whether the computer is powered on or off.
2. Remove the PCMCIA slot cover, if any, on the computer.
3. Insert the DAQCard-6715 into the PCMCIA slot and attach the I/O cable. The DAQCard has two connectors—a 68-pin PCMCIA bus connector on one end and a 68-pin I/O connector on the other end. Insert the PCMCIA bus connector into any available Type II PCMCIA slot until the connector is firmly seated. The DAQCard and I/O cable are both designed so that you can attach the cable only one way.

Notes Be careful not to put strain on the I/O cable when inserting it into or removing it from the DAQCard-6715. Always grasp the cable by the connector you are plugging or unplugging. *Never* pull directly on the I/O cable to unplug it from the DAQCard.

You can connect the DAQCard-6715 to 68- and 50-pin accessories. You can use either a SHC68-68-EP or SHC68U-68-EP cable with the DAQCard-6715.

4. Tighten the jackscrews to secure the cable to the DAQCard-6715.

The DAQCard-6715 is now installed.

You are now ready to configure the software for the NI 671*X*/673*X*.

Configuring the NI 671*X*/673*X*

Because of the NI standard architecture for data acquisition, the PCI bus specification, and the PCMCIA (PC Card) specification, the NI 671*X*/673*X* is completely software configurable. Two types of configuration are performed on the NI 671*X*/673*X*: bus-related and data acquisition-related configuration.

The PCI-671*X*/673*X* is fully compatible with the industry-standard *PCI Local Bus Specification Revision 2.2*. This compatibility allows the PCI system to automatically perform all bus-related configurations without user interaction. Bus-related configuration includes setting the device base memory address and interrupt channel.

The PXI-671*X*/6733 device is fully compatible with the industry standard, *PXI Specification Revision 2.0*. This compatibility allows the PXI/CompactPCI system to automatically perform all bus-related configurations, such as setting the device base memory address and interrupt channel, without user interaction.

Data acquisition-related configuration, which you must perform, includes such settings as AI coupling and range, and others. You can modify these settings using NI-DAQ or application-level software, such as LabVIEW and Measurement Studio.

To configure the device in Measurement & Automation Explorer (MAX), refer to either the *DAQ Quick Start Guide* or the *NI-DAQ User Manual for PC Compatibles* at `ni.com/manuals`.

3

Hardware Overview

This chapter presents an overview of the NI 671*X*/673*X* hardware functions. Figure 3-1 shows a block diagram of the NI 6711/6713. Figure 3-2 shows a block diagram of the NI 6715. Figure 3-3 shows a block diagram of the NI 673*X*.

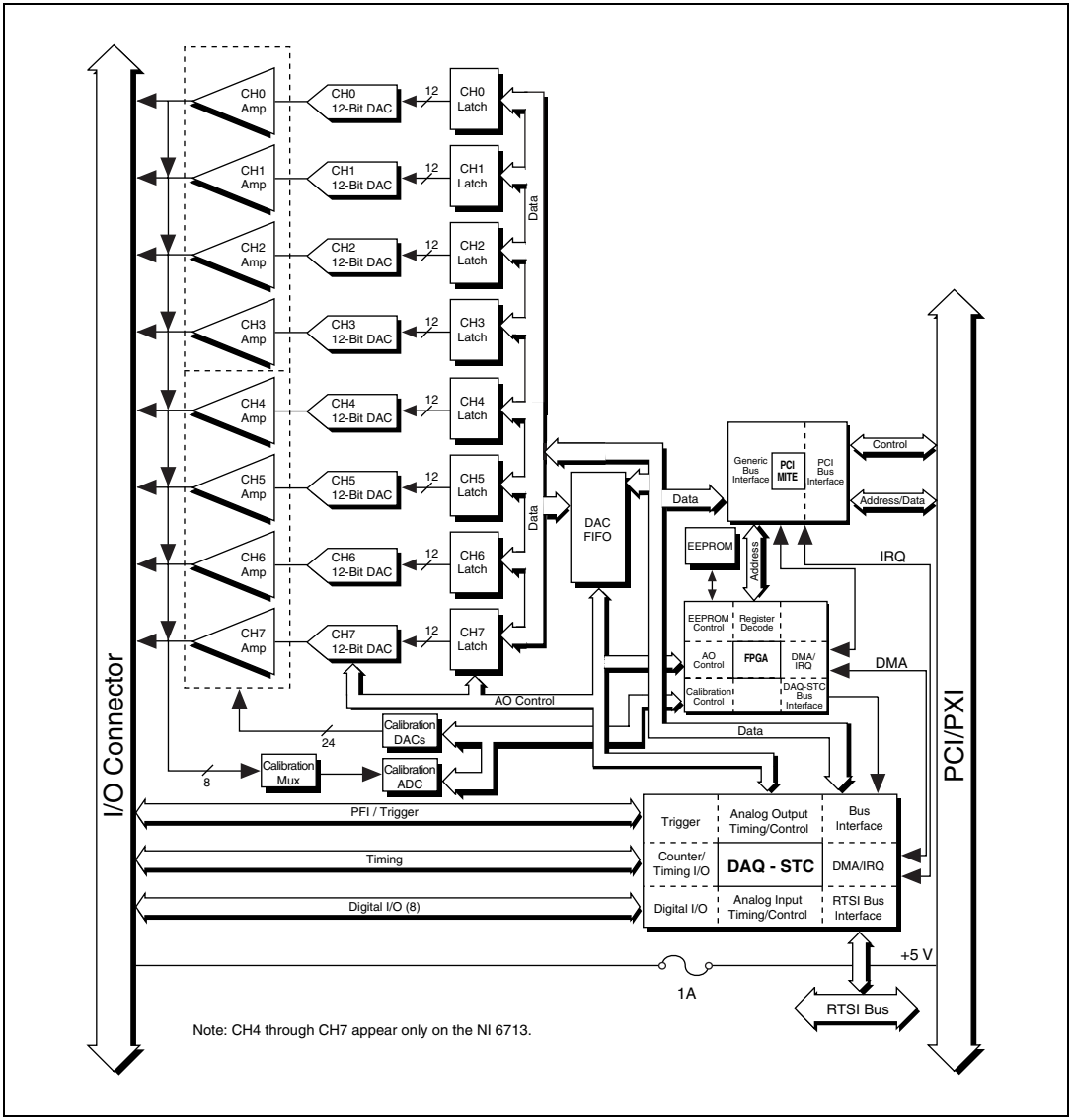


Figure 3-1. NI 6711/6713 Block Diagram

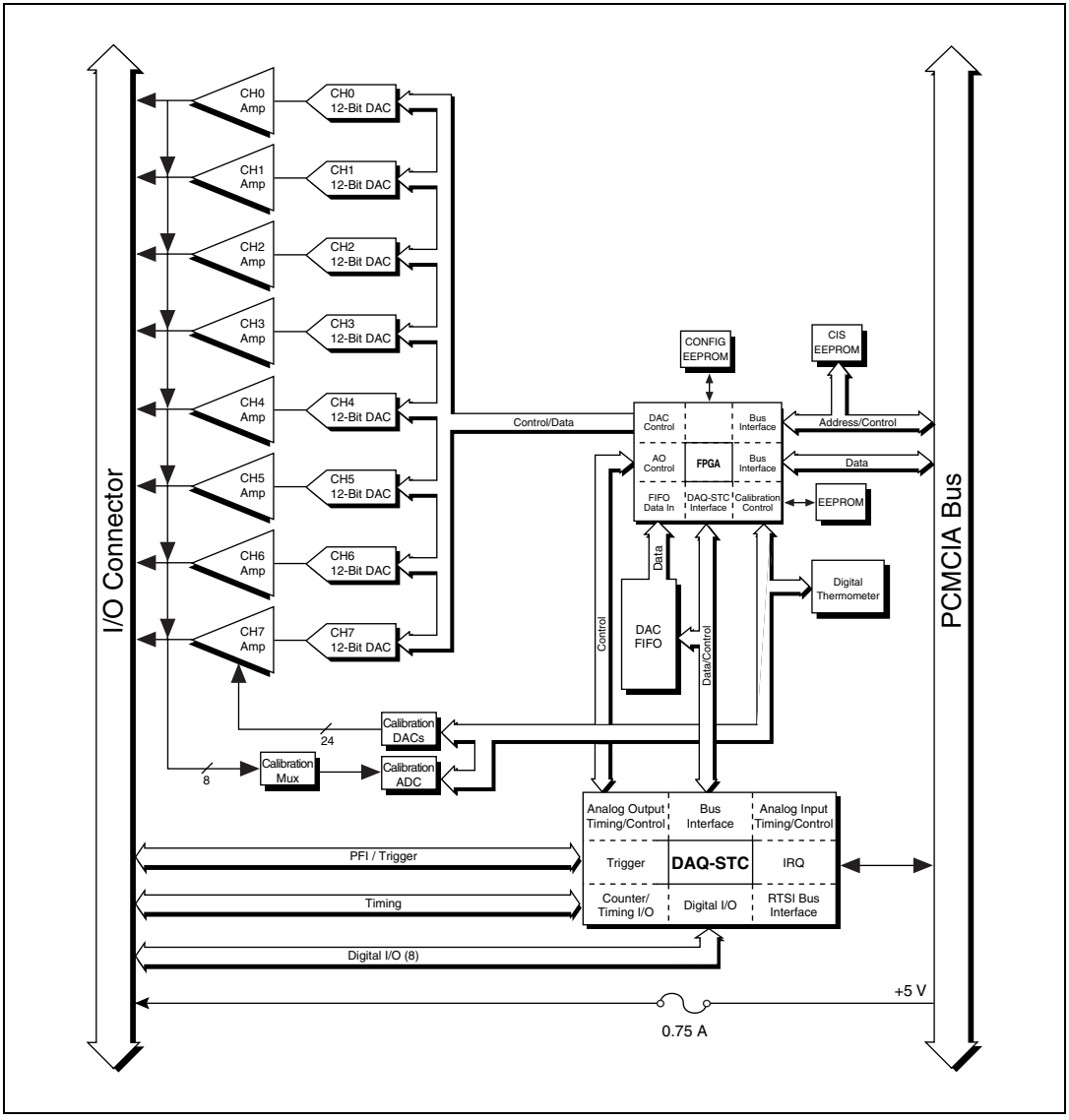


Figure 3-2. NI 6715 Block Diagram

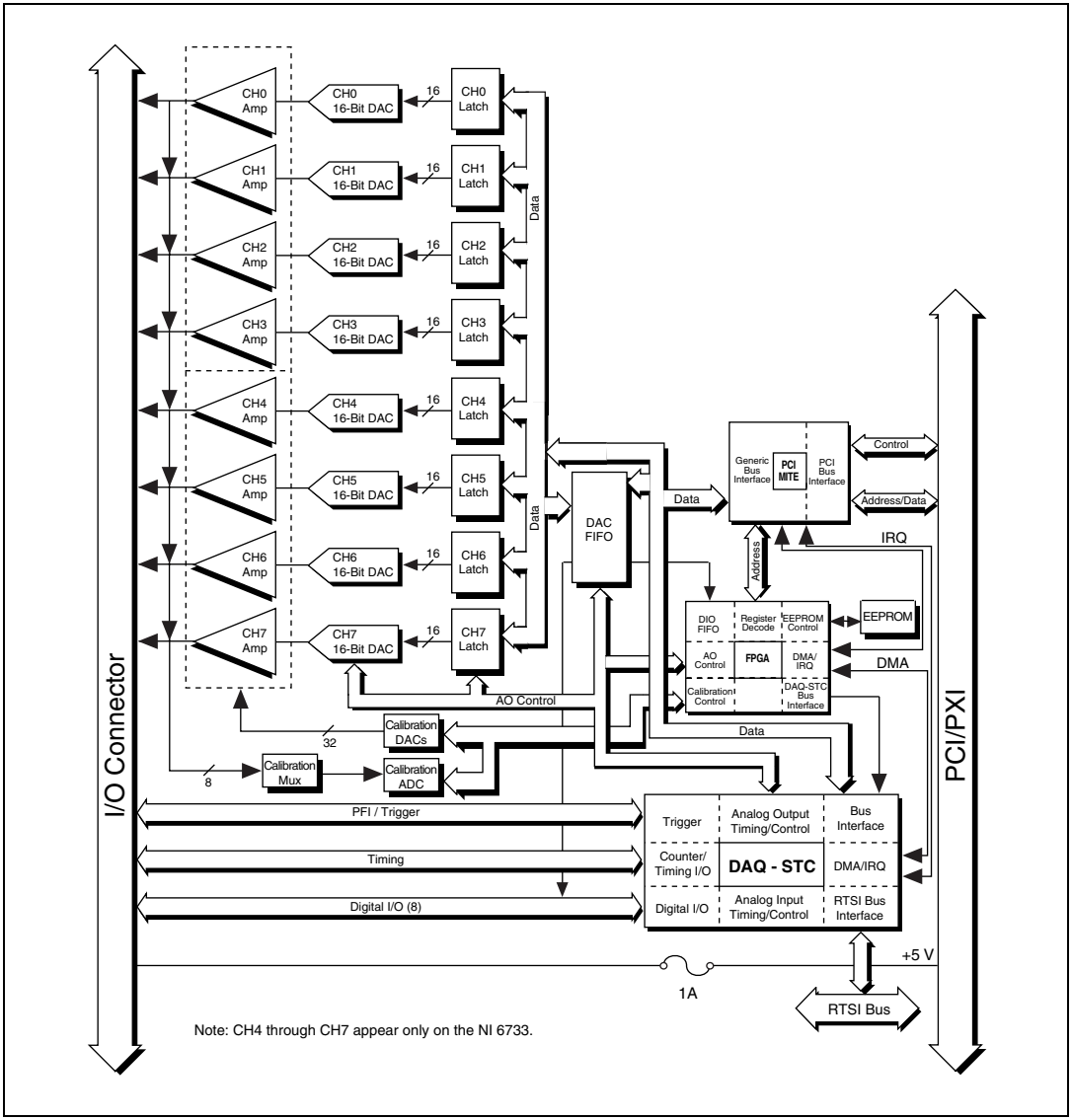


Figure 3-3. NI 673*X* Block Diagram

Analog Output

The NI 6711/6731 has four channels of voltage output at the I/O connector, and the NI 6713/6715/6733 has eight such channels. The reference for the AO circuitry is software-selectable per channel. The reference can be either internal or external, but the range is always bipolar. This means that you can output signals up to ±10 V with internal reference selected or ±EXTREF voltage with external reference selected.

Analog Output Reference Selection

You can connect each DAC to the internal reference of 10 V or to the external reference signal connected to the external reference (EXTREF) pin on the I/O connector. The signal applied to EXTREF should be within ±11 V of AOGND. You can configure each channel to use either internal or external reference. The default reference value selection is internal reference.

Analog Output Reglitch Selection

- NI 671*X* only

In normal operation, a DAC output glitches whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each AO channel contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. This reglitch circuit does *not* eliminate the glitches; it only makes them more uniform in size. By default, reglitching is disabled for all channels; however, you can use NI-DAQ to independently enable reglitching for each channel.

Digital I/O

The NI 671*X*/673*X* contains eight lines of DIO for general-purpose use. You can individually software configure each line for either input or output. At system startup and reset, the DIO ports are all high-impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the counters. The up/down control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

- NI 673*X* only

  The NI 673*X* includes FIFOs for buffered operation. With buffered operation, you can read/write an array of data, using either an internal or external clock source, at a maximum rate of 10 MHz. In addition, you can correlate the DIO and AO operations to the same clock. Refer to the *Connecting Digital I/O Signals* section in Chapter 4, *Connecting the Signals*, for information on which signals you can use to clock the DIO operations. At system startup and reset, the DIO ports are all high-impedance.

  The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the counters. The up/down control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The NI 6711/6713/673*X* uses the RTSI bus to interconnect timing signals between PCI/PXI/CompactPCI devices, and the NI 671*X*/673*X* uses the programmable function input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the NI 671*X*/673*X* to both control and be controlled by other devices and circuits.

There are 13 timing signals internal to the DAQ-STC that you can control with an external source. You can also control these timing signals with signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the UPDATE* signal is shown in Figure 3-4.

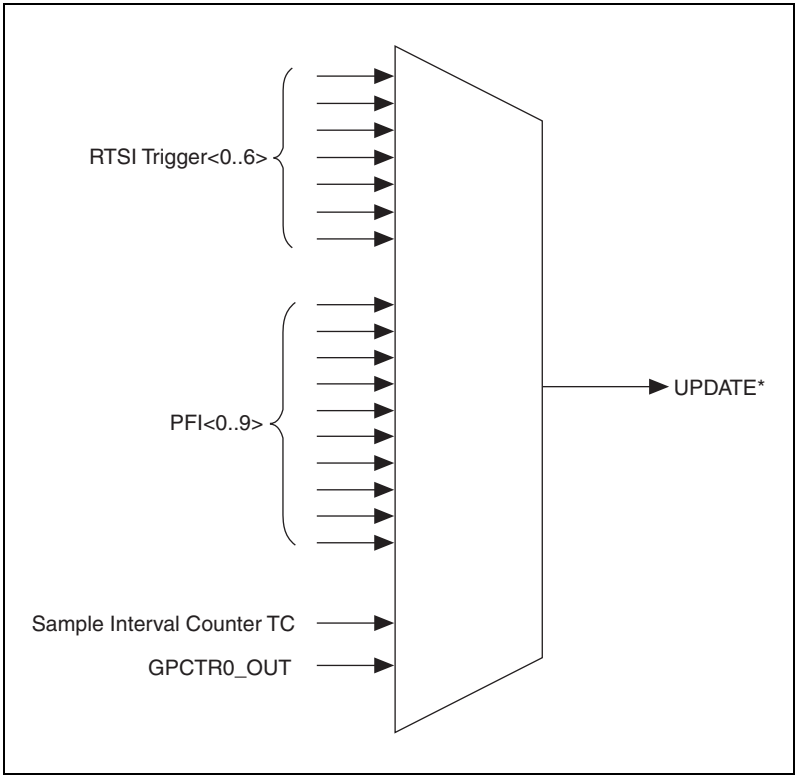


Figure 3-4. UPDATE* Signal Routing

Figure 3-4 shows that you can generate UPDATE* from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section, and on the PFI pins, as indicated in the *Programmable Function Input Connections* section in Chapter 4, *Connecting the Signals*.

NI-DAQ routes signals using the Route Signal VI in LabVIEW and the `Select_Signal` function in other programming languages. Refer to the *LabVIEW Help* or the *NI-DAQ Function Reference Help* for more information about these functions.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select a PFI as the external source for a given timing signal. It is important to note that you can use any PFI as an input by any of the timing signals and that multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can also individually enable each PFI pin to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

- NI 6711/6713/673*X* only

Many functions performed by the NI 6711/6713/673*X* require a frequency timebase to generate the necessary timing signals for controlling DAC updates or general-purpose signals at the I/O connector.

The NI 6711/6713/673*X* can use either the internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the device to use the internal timebase, which is software-selectable, you can program the device to drive the internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used by the device as the primary frequency source. The default configuration is to use the internal timebase without driving the RTSI bus timebase signal.

RTSI Triggers

- NI 6711/6713/673*X* only

The seven RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for the NI 6711/6713/673*X* devices sharing the RTSI bus. These bidirectional lines can drive any of five timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-5.

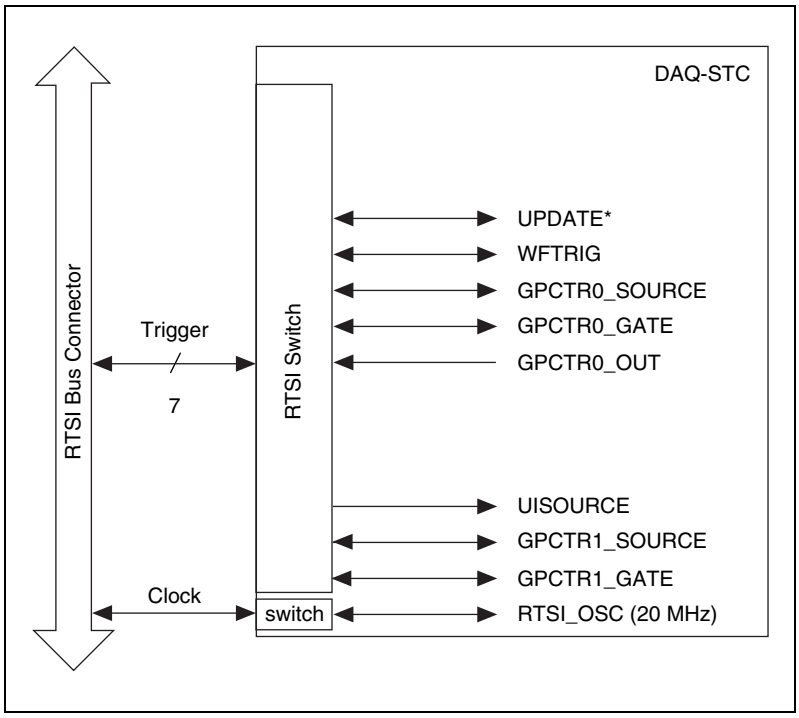


Figure 3-5. RTSI Bus Signal Connection

Refer to the *Connecting the Timing Signals* section in Chapter 4, *Connecting the Signals*, for a description of the signals.

4

Connecting the Signals

This chapter describes how to make input and output signal connections to the NI 671*X*/673*X* through the device I/O connector. SH68-68-EP or similar 68-pin shielded cable. Table 4-1 shows the cables that can be used with the I/O connectors to connect to different accessories.

Table 4-1. I/O Connector Details

Device with I/O Connector	Number of Pins	Cable for Connecting to 100-pin Accessories	Cable for Connecting to 68-pin Accessories
NI 6711/6713/673*X*	68	N/A	SH68-68-EP or similar 68-pin shielded cable
NI 6715	68	N/A	SHC68-68-EP, SHC68U-68-EP, or similar 68-pin shielded cables

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the NI 671*X*/673*X*. Figure 4-2 shows the pin assignments for the 50-pin I/O cable connector when used with the NI 671*X*/673*X*. Signal descriptions follow the connector pinouts.

AOGND	34	68	NC
NC	33	67	AOGND
AOGND	32	66	AOGND
AOGND	31	65	DAC7OUT[1]
DAC6OUT[1]	30	64	AOGND
AOGND	29	63	AOGND
DAC5OUT[1]	28	62	NC
AOGND	27	61	AOGND
AOGND	26	60	DAC4OUT[1]
DAC3OUT	25	59	AOGND
AOGND	24	58	AOGND
AOGND	23	57	DAC2OUT
DAC0OUT	22	56	AOGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	NC
PFI0	11	45	NC
PFI1	10	44	DGND
DGND	9	43	PFI2
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] No Connect on the NI 6711/6731

Figure 4-1. 68-Pin I/O Connector Pin Assignment for the NI 671*X*/673*X*

AOGND	1	2	AOGND
NC	3	4	AOGND
NC	5	6	AOGND
DAC7OUT[1]	7	8	AOGND
DAC6OUT[1]	9	10	AOGND
DAC5OUT[1]	11	12	AOGND
DAC4OUT[1]	13	14	AOGND
DAC3OUT	15	16	AOGND
DAC2OUT	17	18	AOGND
NC	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5 V
+5 V	35	36	NC
NC	37	38	NC
NC	39	40	NC
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	NC
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

[1]No Connect on the NI 6711/6731

Figure 4-2. 50-Pin I/O Connector Pin Assignment for the NI 671*X*/673*X*

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 671*X*/673*X* can damage the device and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table 4-3. NI is *not* liable for any damage resulting from signal connections that exceed the maximum ratings.

I/O Connector Signal Descriptions

Table 4-2. Signal Descriptions for I/O Connector Pins

Signal Name	Reference	Direction	Description
AOGND	—	—	Analog Output Ground—The AO voltages and the external reference voltage are referenced to this node.
DAC<0..7>OUT	AOGND	Output	Analog Output Channels 0 through 7—These pins supply the voltage output of the respective channel.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply.
DIO<0..7>	DGND	Input or Output	Digital I/O Signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A (0.75 A, DAQCard-6715)[1] of +5 V supply. The fuse is self-resetting.
EXTREF	AOGND	Input	External Reference—This is the external reference input for the AO circuitry.
PFI0	DGND	Input	PFI0—As an input, this is a PFI. PFI signals are explained in the *Connecting the Timing Signals* section later in this chapter. PFI0 cannot be an output.
PFI1	DGND	Input	PFI1—As an input, this is a PFI. PFI1 cannot be an output.
PFI2	DGND	Input	PFI2—As an input, this is a PFI. PFI2 cannot be an output.
PFI3/GPCTR1_SOURCE	DGND	Input Output	PFI3/Counter 1 Source—As an input, this is a PFI. The default input is Counter 1 Source. As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input Output	PFI4/Counter 1 Gate—As an input, this is a PFI. The default input function is Counter 1 Gate. As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.

Table 4-2. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input Output	PFI5/Update—As an input, this is a PFI. The default input function is the AO UPDATE* signal. As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the AO waveform generation group is being updated.
PFI6/WFTRIG	DGND	Input Output	PFI6/Waveform Trigger—As an input, this is a PFI. The default input function is the AO Waveform Trigger. As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7	DGND	Input	PFI7—As an input, this is a PFI. PFI7 cannot be an output.
PFI8/GPCTR0_SOURCE	DGND	Input Output	PFI8/Counter 0 Source—As an input, this is one of the PFIs. The default input function is the Counter 0 Source. As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input Output	PFI9/Counter 0 Gate—As an input, this is a PFI. The default input function is the general-purpose Counter 0 Gate. As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

[1] The +5 V line on the connector of the DAQCard-6715 is fused at 0.75 A; however, the actual current available can be limited below this value by the host computer. NI recommends limiting current from this line to 250 mA.

Table 4-3. I/O Signal Summary for the NI 671*X*/673*X*

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)/ Slew Rate	Bias
DAC<0..7>OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10 (total not to exceed 20 mA total for all 8 outputs combined, DAQCard –6715)	5 at –10	20 V/µs, NI 671*X* 20 V/µs, NI 673*X*	—
AOGND	AO	—	—	—	—	—	—
DGND	DIO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1 A (0.75 A, DAQCard –6715)[1]	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu
EXTREF	AI	10 kΩ	25/15	—	—	—	—
PFI0	DI	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pd
PFI1	DI	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2	DI	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-3. I/O Signal Summary for the NI 671*X*/673*X* (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)/ Slew Rate	Bias
PFI7	DI	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

[1] The +5 V line on the connector of the DAQCard-6715 is fused at 0.75 A; however, the actual current available can be limited below this value by the host computer. NI recommends limiting current from this line to 250 mA.

pd = pull-down; pu = pull-up; DO = Digital Output

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual values may range between 17 and 100 kΩ.

Connecting Analog Output Signals

The AO signals are DAC<0..7>OUT, AOGND, and EXTREF.

DAC0OUT is the voltage output signal for AO channel 0.

EXTREF is the external reference input for all AO channels. You can use this input to reduce the voltage swing on the DAC outputs while preserving the dynamic range. For example, with internal reference the least significant bit (LSB), or the minimal change, on a voltage output on the NI 671*X* is as follows:

$$\frac{20\text{ V}}{4{,}096} = 4.88\text{ mV}$$

For an external reference at 5 V, you can output ±5 V with the LSB on a voltage output reduced to 2.44 mV. This gives you a higher resolution at lower voltage.

The LSB on a voltage output on the NI 673*X* is as follows:

$$\frac{20\ \text{V}}{65{,}536} = 305.1\ \mu\text{V}$$

For an external reference at 5 V, you can output ±5 V with the LSB on a voltage output reduced to 152.5 µV. This gives you a higher resolution at lower voltage.

You must individually configure each AO channel for external reference selection so that the signal applied at the external reference input can be used by that channel. If you do not specify an external reference, the channel uses the internal reference. AO configuration options are explained in the *Analog Output* section in Chapter 3, *Hardware Overview*.

The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for the AO channels. DAC<0..7>OUT and EXTREF are referenced to AOGND.

The external reference signal can be either a DC or an AC signal. The device multiplies this reference signal by the DAC code that is divided by the full-scale DAC code, to generate the output voltage.

Figure 4-3 shows how to make analog output connections to the NI 671*X*/673*X* device.

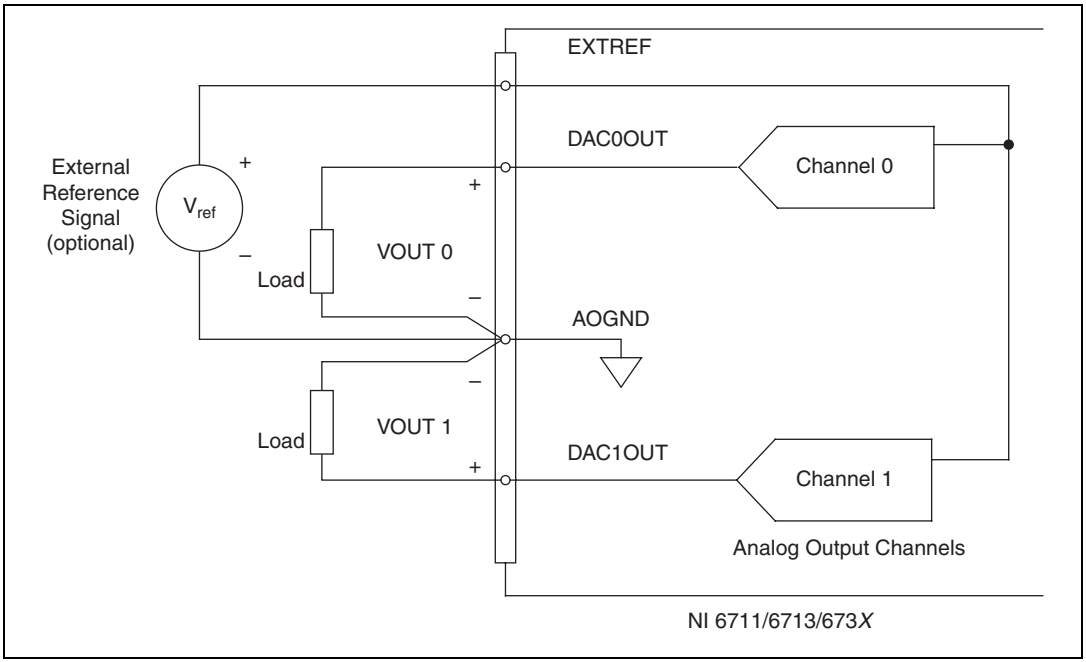


Figure 4-3. Analog Output Connections

Connecting Digital I/O Signals

The DIO signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can individually program each line as an input or output.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the NI 671*X*/673*X* and the computer. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-4 shows signal connections for three typical digital I/O applications.

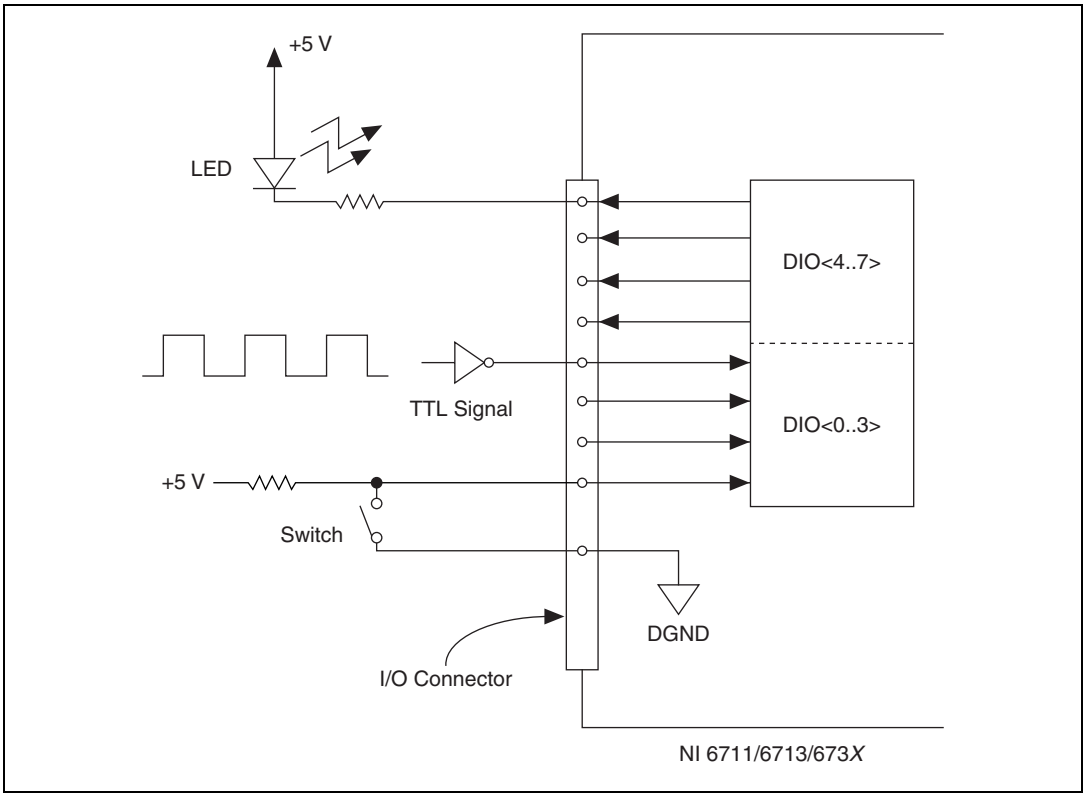


Figure 4-4. Digital I/O Connections

Figure 4-4 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the switch state shown in Figure 4-4. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in Figure 4-4.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

Connecting the Power

Two pins on the I/O connector supply +5 V from the computer power supply through a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. You can use these pins, referenced to DGND, to power external digital circuitry.

Power rating: +4.65 to +5.25 VDC at 1 A (0.75 A for the DAQCard-6715)[1]

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the NI 671*X*/673*X* or any other device. Doing so can damage the NI 671*X*/673*X* and the computer. NI is *not* liable for damage resulting from such a connection.

Connecting the Timing Signals

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the NI 671*X*/673*X* and the computer. NI is *not* liable for any damage resulting from such signal connections.

All external control over the timing of the NI 671*X*/673*X* is routed through the 10 PFIs labeled PFI0 through PFI9. These signals are explained in detail in the *Programmable Function Input Connections* section. On the NI 671*X*/673*X*, six PFIs are bidirectional and four PFIs are input only (PFI0, PFI1, PFI2, PFI7). As outputs these PFIs are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are four other dedicated outputs for the remainder of the timing signals (SCANCLK is not used on the NI 671*X*/673*X*). As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The waveform generation signals are explained in the *Waveform Generation Timing Connections* section. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section.

[1] The +5 V line on the connector of the DAQCard-6715 is fused at 0.75 A; however, the actual current available can be limited below this value by the host computer. NI recommends limiting current from this line to 250 mA.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-5, which shows how to connect an external PFI0 source and an external PFI2 source to two PFI pins on the NI 671*X*/673*X*.

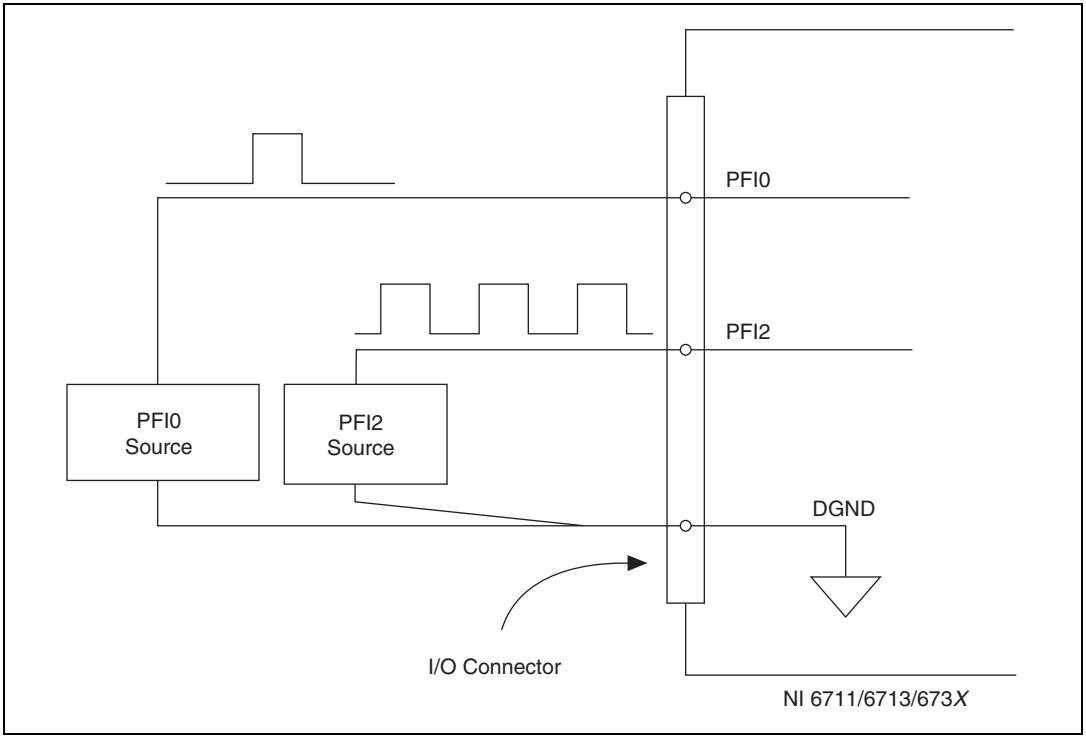


Figure 4-5. Timing I/O Connections

Programmable Function Input Connections

There are seven internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software-selectable from any PFI. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for applications requiring alternative wiring.

You can individually enable six of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

Note Be careful not to drive a PFI signal externally when it is configured as an output.

When using the PFI pin as an input, you can individually configure each PFI for edge or level detection and for polarity selection. You can use the polarity selection for any of the seven timing signals, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there can be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

Waveform Generation Timing Connections

The analog group defined for the NI 671*X*/673*X* is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, WFTRIG is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of WFTRIG starts the waveform generation for the DACs. The update interval counter (UI) is started if you select the internally generated UPDATE* signal.

As an output, WFTRIG reflects the trigger that initiates waveform generation, even if the waveform generation is externally triggered by another PFI. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to high-impedance at startup.

Figures 4-6 and 4-7 show the input and output timing requirements for WFTRIG.

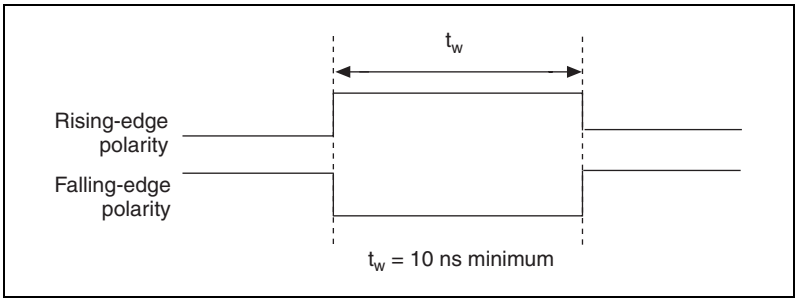


Figure 4-6. WFTRIG Input Signal Timing

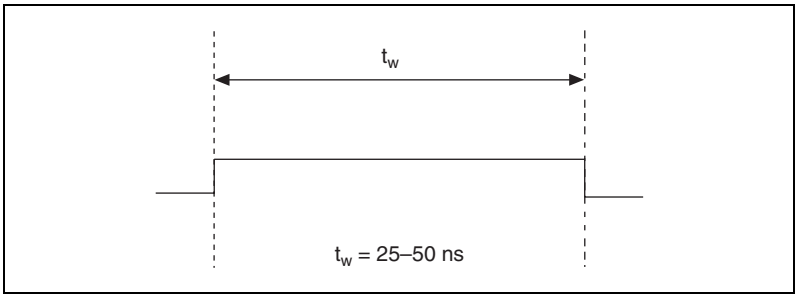


Figure 4-7. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, UPDATE* is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of UPDATE* updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, UPDATE* reflects the actual update pulse that is connected to the DACs, even if the updates are externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 75 ns. This output is set to high-impedance at startup.

Figures 4-8 and 4-9 show the input and output timing requirements for the UPDATE* signal.

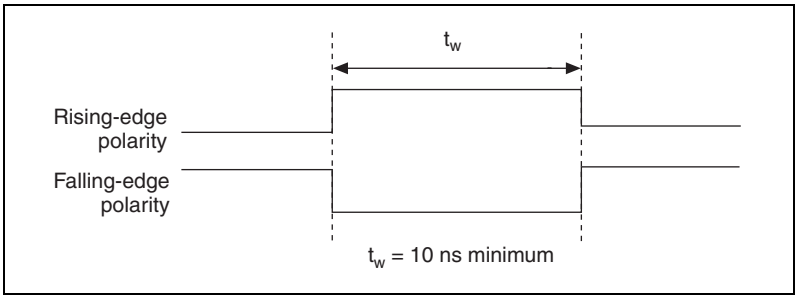


Figure 4-8. UPDATE* Input Signal Timing

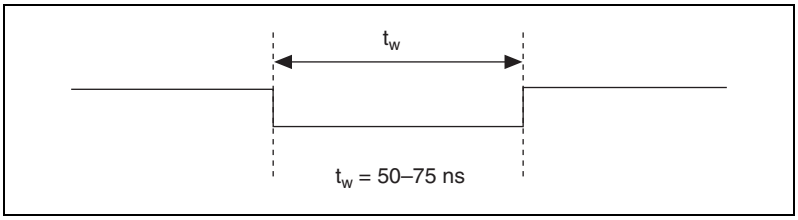


Figure 4-9. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The UI on the NI 671*X*/673*X* normally generates UPDATE* unless you select some external source. UI is started by the WFTRIG signal and can be stopped by software or the internal buffer counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. UI uses UISOURCE as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for UISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

Figure 4-10 shows the timing requirements for UISOURCE.

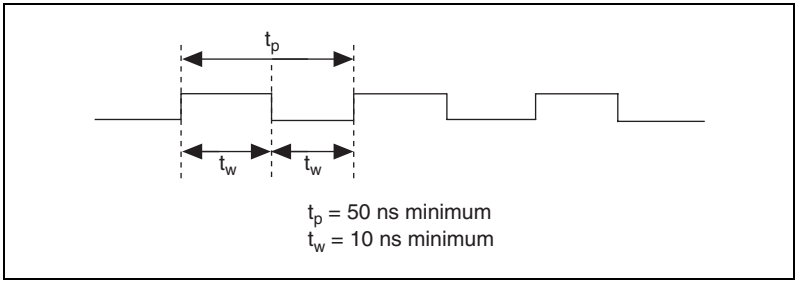


Figure 4-10. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

Unless you select some external source, either the 20 MHz or 100 kHz internal timebase generates UISOURCE.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, GPCTR0_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR0_SOURCE reflects the actual clock connected to general-purpose counter 0, even if another PFI is externally inputting the source clock. This output is set to high-impedance at startup.

Figure 4-11 shows the timing requirements for GPCTR0_SOURCE.

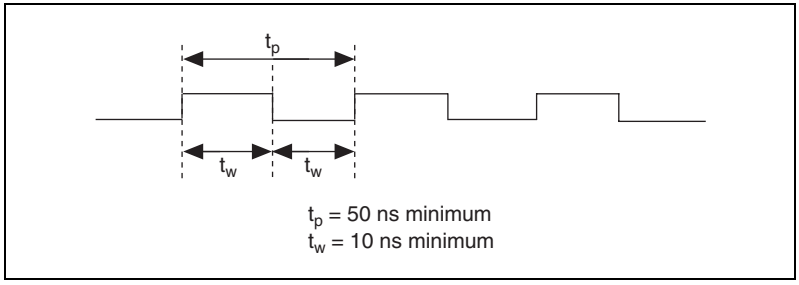


Figure 4-11. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

Unless you select some external source, the 20 MHz or 100 kHz timebase generates GPCTR0_SOURCE.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, GPCTR0_GATE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, GPCTR0_GATE reflects the actual gate signal connected to general-purpose counter 0, even if the gate is externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-12 shows the timing requirements for GPCTR0_GATE.

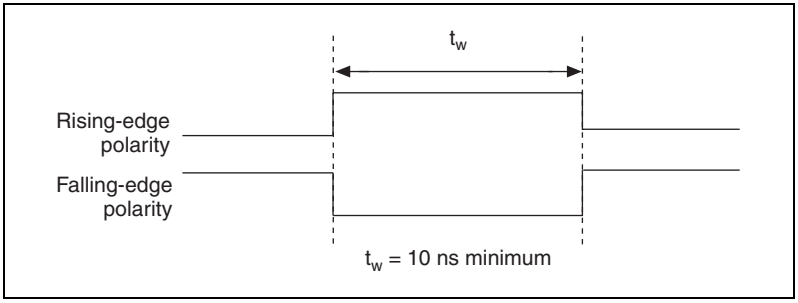


Figure 4-12. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. GPCTR0_OUT reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup.

Figure 4-13 shows the timing of GPCTR0_OUT.

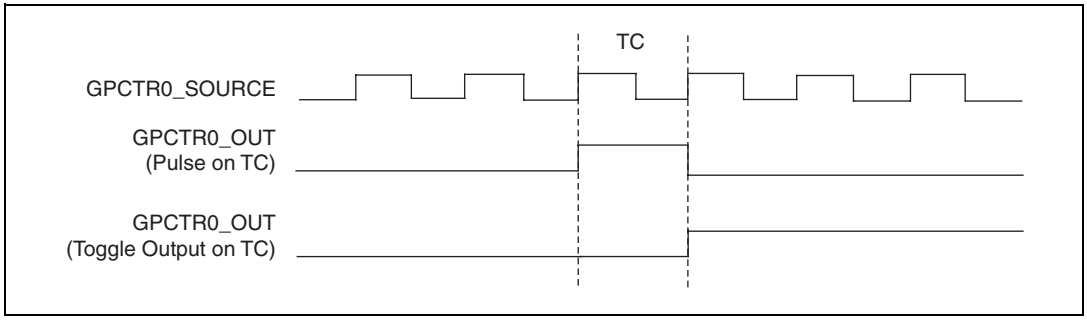


Figure 4-13. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

You can externally input this signal on the DIO6 pin, but it is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and counts up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, GPCTR1_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if the source clock is externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-14 shows the timing requirements for GPCTR1_SOURCE.

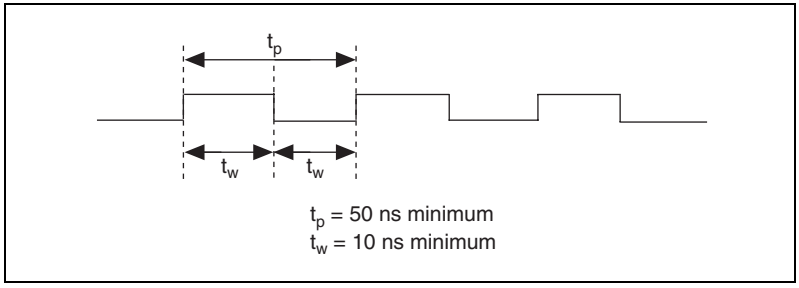


Figure 4-14. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, GPCTR1_GATE is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform such actions as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1, even if the gate is externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-15 shows the timing requirements for the GPCTR1_GATE signal.

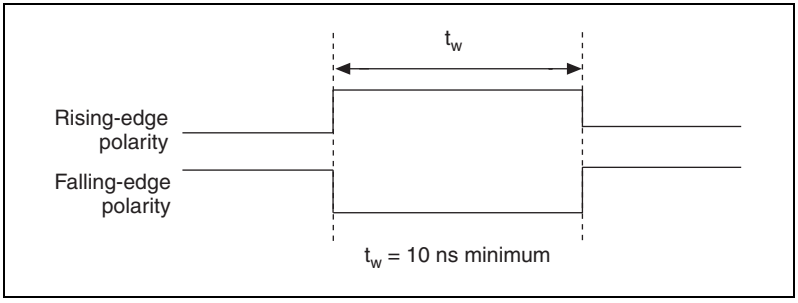


Figure 4-15. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This output is set to high-impedance at startup.

Figure 4-16 shows the timing requirements for the GPCTR1_OUT signal.

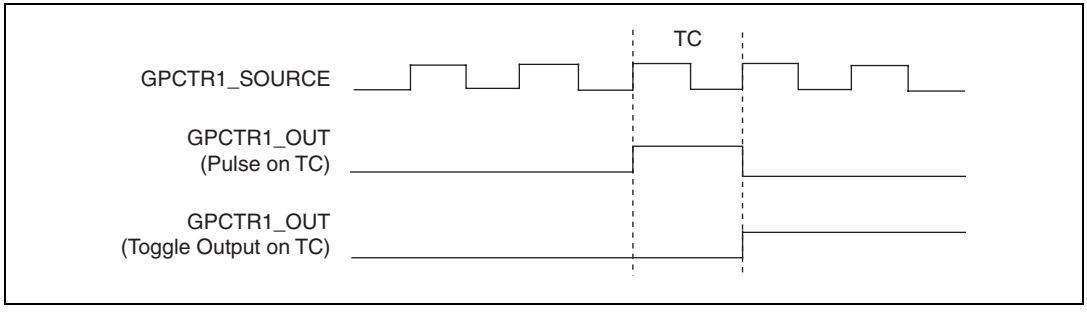
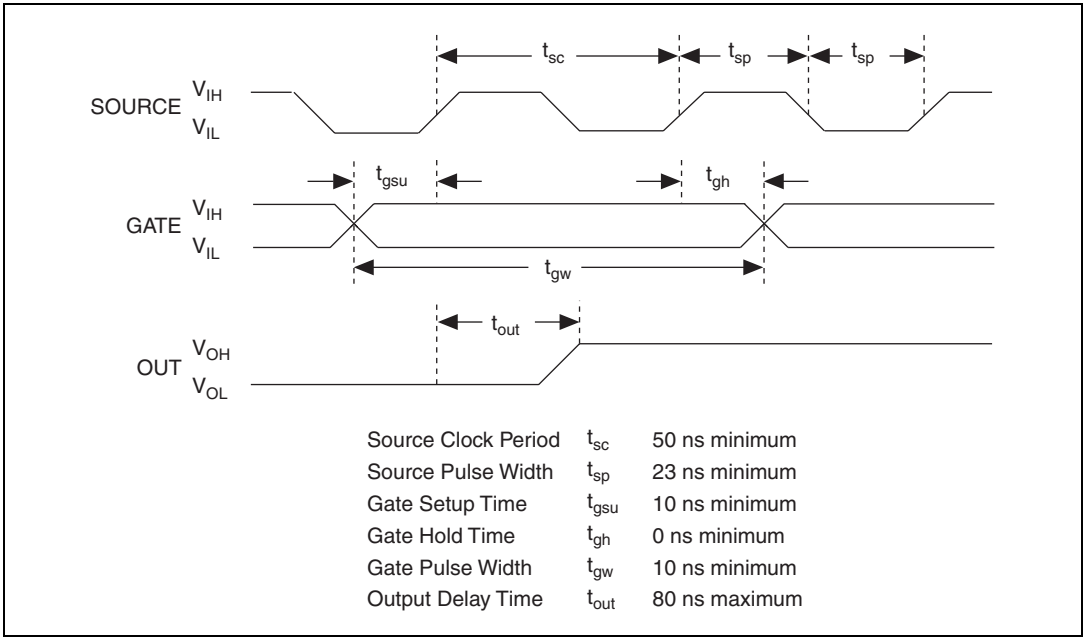


Figure 4-16. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

You can externally input this signal on the DIO7 pin, but it is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-17 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals on the NI 6711/6713/673*X*.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-17. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-17 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the NI 6711/6713/673*X*. Figure 4-17 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal so that

the gate can take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-17. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, you cannot synchronize the gate signal with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the NI 671*X*/673*X*. Figure 4-17 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The frequency generator for the NI 671*X*/673*X* outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software-selectable. This output is set to high-impedance at startup.

Field Wiring Considerations

The following recommendations apply for all signal connections to the NI 671*X*/673*X*:

- Separate the signal lines of the NI 671*X*/673*X* from high-current or high-voltage lines. These lines can induce currents in or voltages on the signal lines of the NI 671*X*/673*X* if they run in close parallel paths. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

Refer to the NI Developer Zone document, *Field Wiring and Noise Consideration for Analog Signals,* at `ni.com/zone` for more information.

5

Calibration

This chapter discusses calibration procedures for the NI 671*X*/673*X*. If you are using NI-DAQ, it includes calibration functions for performing all the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the NI 671*X*/673*X*, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for most applications. If you do not calibrate the device, the signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate. The last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI 671*X*/673*X* is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM, there is a user-modifiable calibration area in addition to the permanent factory calibration area, so you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

The loading factory calibration constants method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. You should self-calibrate when the device is installed in the environment in which it will be used.

Self-Calibration

The NI 671*X*/673*X* can measure and correct for almost all of its calibration-related errors without any external signal connections. NI-DAQ provides a self-calibration method. This self-calibration process, which generally takes less than five minutes, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements and you can ignore a small[1] amount of gain error, self-calibration should be sufficient.

External Calibration

The NI 671*X*/673*X* has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using the device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate the device.

[1] The onboard voltage reference has a temperature coefficient of 5 ppm/°C max (25 µV/°C) on the NI 671*X* or 0.6 ppm/°C max (3 µV/°C) on the NI 673*X*. Therefore, if the temperature difference between the factory calibration and the service environment is less than 10 °C, the maximum gain error at full scale output is less than 50 ppm, 0.005 percent on the NI 671*X* or 6 ppm, 0.0006 percent on the NI 673*X*, after performing self-calibration.

An external calibration refers to calibrating the device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process, and since you can save the results in the EEPROM, you should not have to perform an external calibration very often. You can externally calibrate the device by calling the `Calibrate_E_Series` function in NI-DAQ.

To externally calibrate the device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. For example, to calibrate a 16-bit device, the external reference should be at least ±0.001% (±10 ppm) accurate.

Note NI recommends using a +5 V external reference voltage when performing calibration.

Other Considerations

The CalDACs adjust the gain error of each AO channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, you cannot calibrate the AO gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the AO channel either in software or with external hardware. Refer to Appendix A, *Specifications*, for AO gain error information.

A

Specifications

This appendix lists the specifications of the NI 671*X*/673*X*. These specifications are typical at 25 °C unless otherwise noted.

Analog Output

Output Characteristics

Number of channels

NI 6713/6715/6733 ..... 8 voltage outputs

NI 6711/6731 ..... 4 voltage outputs

Resolution

NI 671*X*..... 12 bits, 1 in 4,096

NI 673*X*..... 16 bits, 1 in 65,536

Max update rate

Number of Channels	Max Update Rate (NI 6711/6713/673*X*)		Max Update Rate (NI 6715)	
	Using Local FIFO (kS/s)[1]	Using Host PC Memory (kS/s)[2]	Using Local FIFO (kS/s)	Using Host PC Memory (kS/s)[3]
1	1,000	1,000	1,000	800
2	1,000	1,000	850	400
3	1,000	1,000	750	266
4	1,000	1,000	650	200
5	1,000	1,000	600	160
6	952	1,000	550	133
7	833	869	510	114
8	740	769	480	100

[1] These numbers apply to continuous waveform generation, which allows for the time it takes to reset the FIFO to the beginning when cycling through it. This additional time, about 200 ns, is not incurred when using host PC memory for waveform generation. Max update rate in FIFO mode does not change regardless of the number of devices in the system.

[2] These results were measured using a PCI-6711/6713 device with a 90 MHz Pentium machine. These numbers may change when using more devices or when other CPU or bus activity occurs.

[3] These results were measured using a DAQCard-6715 with a 266 MHz Pentium II machine. These numbers may change when using more devices or when other CPU or bus activity occurs.

Type of DAC

NI 6711/6713/673*X* .....Double buffered, multiplying

NI 6715 .....Serial, multiplying

FIFO buffer size

NI 6711/6731 .....8,192 samples

NI 6713/6733 .....16,384 samples

NI 6715 .....8,192 samples

Data transfers .....DMA (NI 6711/6713/673*X* only), interrupts, programmed I/O

DMA modes .....Scatter gather (NI 6711/6713/673*X* only)

Accuracy Information

Nominal Range (V)	Absolute Accuracy for the NI 671*X*				
	% of Reading			Offset	Temp Drift
Full Scale	24 Hours	90 Days	1 Year	(mV)	(%/°C)
±10	0.0177%	0.0197%	0.0219%	±5.933	0.0005%

Absolute accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage)

Note: Temp drift applies only if ambient is greater than ±10 °C of previous external calibration.

Nominal Range (V)	Absolute Accuracy for the NI 673*X*				
	% of Reading			Offset	Temp Drift
Full Scale	24 Hours	90 Days	1 Year	(µV)	(%/°C)
±10	0.0044%	0.0052%	0.0061%	±1,026.97	0.00006%

Absolute accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage)

Note: Temp drift applies only if ambient is greater than ±10 °C of previous external calibration.

Transfer Characteristics

Relative accuracy (INL)

After calibration

NI 671*X*..... ±0.3 LSB typ, ±0.5 LSB max

NI 673*X*..... ±2.2 LSB max

Before calibration

NI 671*X*..... ±4.0 LSB max

NI 673*X*..... ±2.2 LSB max

DNL

After calibration

NI 671*X*..... ±0.3 LSB typ, ±1.0 LSB max

NI 673*X*..... ±1.0 LSB max

Before calibration

NI 671*X*..... ±3.0 LSB max

NI 673*X*..... ±1.0 LSB max

Monotonicity

NI 671*X* .....12 bits guaranteed after calibration

NI 673*X* .....16 bits guaranteed after calibration

Offset error

After calibration

NI 671*X* .....±1.0 mV typ, ±5.9 mV max

NI 673*X* .....±168 µV max

Before calibration

NI 671*X* .....±200 mV max

NI 673*X* .....±40 mV max

Gain error (relative to internal reference)

After calibration

NI 671*X* .....±0.01% of output max

NI 673*X* .....±30 ppm of output max

Before calibration

NI 671*X* .....±0.5% of output max

NI 673*X* .....±9,000 ppm of output max

Gain error

NI 671*X*
(relative to external reference).....+0.0 to +0.67% of output max, not adjustable at > 4 V

NI 673*X*
(relative to external reference).....±0.1% of output max, not adjustable

Voltage Output

Ranges .....±10 V, ±EXTREF

Output coupling .....DC

Output impedance.....0.1 Ω max

Current drive.....±5 mA max (for the NI 6715, total not to exceed 20 mA for all 8 outputs combined)

Output stability ..... Any passive load, up to 1,500 pF

Protection ..... Short-circuit to ground

Power-on state ..... 0 V

External Reference Input

Range ..... ±11 V

Overvoltage protection ..... ±25 V powered on,
±15 V powered off

Input impedance

- NI 671*X* ..... 10 kΩ
- NI 673*X* ..... 1 MΩ

Bandwidth (–3 dB) ..... 1 MHz

Dynamic Characteristics

Slew rate

- NI 671*X* ..... 20 V/µs
- NI 673*X* ..... 15 V/µs

Noise

- NI 6711/6713 ..... 200 μV_{rms}, DC to 1 MHz
- NI 6715 ..... 400 μV_{rms}, DC to 1 MHz
- NI 673*X* ..... 80 μV_{rms}, DC to 1 MHz

Channel crosstalk

- NI 6711/6713 ..... –70 dB with SH68-68-EP cable (generating a 10 V, 10 point sinusoidal at 100 kHz on the reference channel)
- NI 6715 ..... –60 dB (generating a 10 V, 10 point sinusoidal at 100 kHz on the reference channel)
- NI 673*X* ..... –95 dB (generating a 10 V, 10 point sinusoidal at 100 kHz on the reference channel)

Settling time

NI 6711/6713 ..... 3.0 µs to ±0.5 LSB accuracy

NI 6715 ..... 5.0 µs to ±0.5 LSB accuracy

NI 673*X* ..... 2.8 µs to ±1.0 LSB accuracy

Total harmonic distortion

NI 671*X* ..... –80 dB typ (generating a 10 V, 1,000 point, 750 Hz sine wave, summing 9 harmonics)

NI 673*X* ..... –90 dB typ (generating a 10 V, 1,000 point, 1 kHz sine wave, summing 9 harmonics)

Stability

Offset temperature coefficient

NI 671*X* ..... ±50 µV/°C

NI 673*X* ..... ±35 µV/°C

Gain temperature coefficient

Internal reference

NI 671*X* ..... ±25 ppm/°C

NI 673*X* ..... ±6.5 ppm/°C

External reference

NI 671*X* ..... ±25 ppm/°C

NI 673*X* ..... ±5.0 ppm/°C

Onboard calibration reference

Level

NI 671*X* ..... 5.000 V (±2.5 mV) (actual value stored in EEPROM)

NI 673*X* ..... 5.000 V (±1.0 mV) (actual value stored in EEPROM)

Temperature coefficient

NI 671*X* ..... ±5.0 ppm/°C max

NI 673*X* ..... ±0.6 ppm/°C max

Long-term stability

NI 671*X* ..... ±15 ppm/$\sqrt{1,000\ \text{h}}$

NI 673*X* ..... ±6.0 ppm/$\sqrt{1,000\ \text{h}}$

Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0.0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state..... Input (high-impedance)

Data transfers

NI 671*X*..... Programmed I/O

NI 673*X*..... DMA, interrupts, programmed I/O

Input buffer ..... 2,000 bytes (NI 673*X*)

Output buffer..... 2,000 bytes (NI 673*X*)

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

Counter/timers ..... 24 bits

Frequency scaler ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

Counter/timers ..... 20 MHz, 100 kHz

Frequency scaler ..... 10 MHz, 100 kHz

Base clock accuracy.....±0.01% over operating temperature

Max source frequency.....20 MHz

Min source pulse duration .....10 ns, edge-detect mode

Min gate pulse duration .....10 ns, edge-detect mode

Data transfers.....DMA (NI 6711/6713/673*X* only), interrupts, programmed I/O

DMA modes .....Scatter-gather (NI 6711/6713/673*X* only)

Triggers

Digital Trigger

Compatibility .....TTL

Response .....Rising or falling edge

Pulse width .....10 ns min

RTSI and PXI Trigger Lines

- PCI-671*X*/673*X*

  Trigger lines<0..6> 7

  RTSI clock.....1

- PXI-671*X*/6733

  Trigger lines<0..5> 6

  Star trigger 1

  Clock.....1

Bus Interface

- PCI-671*X*/673*X*
  Type ..... 5 V PCI master, slave
- PXI-671*X*/6733
  Type ..... PXI/CompactPCI master, slave
- DAQCard-6715
  Type ..... 16-bit PC Card (PCMCIA)

Power Requirement

NI 6711

+5 VDC (±5%)..... 0.80 A typ, 1.0 A max

Power available at I/O connector.... +4.65 to +5.25 VDC at 1 A

NI 6713

+5 VDC (±5%)..... 1.25 A typ, 1.5 A max

Power available at I/O connector.... +4.65 to +5.25 VDC at 1 A

NI 6715

+5 VDC (±5%)..... 160 mA typ,
250 mA max plus any current
used from the I/O connector

NI 6731

+5 VDC (±5%)..... 0.80 A typ, 1.25 A max

+3.3 VDC (±5%)..... 125 mA typ, 250 mA max

Power available at I/O connector.... +4.65 to +5.25 VDC at 1 A

NI 6733

+5 VDC (±5%)..... 1.25 A typ, 1.8 A max

+3.3 VDC (±5%)..... 125 mA typ, 250 mA max

Power available at I/O connector.... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions (not including connectors)

NI 671*X*/673*X* for PCI .....17.5 by 10.7 cm (6.87 by 4.2 in.)

NI 671*X*/6733 for PXI/CompactPCI .....16 by 10 cm (6.3 by 3.9 in.)

NI 6715 .....Type II PC Card

I/O connector

NI 671*X*/673*X* .....68-pin male SCSI-II type

NI 6715 .....68-pin female Honda connector

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth .....±11 V, Installation Category I

Channel-to-channel.....±22 V, Installation Category I

Environmental

Operating temperature .....0 to 50 °C

Storage temperature .....–55 to 150 °C

Humidity .....5 to 90% RH, noncondensing

Maximum altitude.....2000 meters

Pollution degree (indoor use only) 2

Safety

The device meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3111-1:1994
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions..... EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity..... Evaluated to EN 61326:1997/
A1:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the DoC for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

B

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of the NI 671*X*/673*X*.

General Information

What is the NI 671*X*/673*X*?

The NI 671*X*/673*X* is a switchless and jumperless analog output device that uses the DAQ-STC for timing.

What is the DAQ-STC?

The DAQ-STC is the system timing control, application-specific integrated circuit (ASIC) designed by NI and is the backbone of the NI 671*X*/673*X*. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- AI—two 24-bit, two 16-bit counters (not used on the NI 671*X*/673*X*)
- AO—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be independently configured with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities include buffered pulse generation and seamless changes to the sampling rate.

What does update rate mean to me?

Update rate is the fastest rate that you can output data from the device and still achieve accurate results. The NI 6711/6713/673*X* has an update rate of 1 MS/s at up to four channels, and the NI 6715 has an update rate of 1 MS/s on one channel and 480 kS/s on all eight channels simultaneously. However, the outputs of the NI 6715 settle to within ±1/2 LSB of their final value within about 5 µs, restricting large-scale accurate outputs to 200 kS/s/channel.

What type of 5 V protection does the NI 671*X*/673*X* have?

The NI 6711/6713/673*X* has 5 V lines equipped with a self-resetting 1 A fuse. The NI 6715 has 5 V lines equipped with a self-resetting 0.75 A fuse.

Can I use SCXI with the NI 671*X*/673*X*? If so, what SCXI modules are supported?

Yes, the NI 671*X*/673*X* can control a single SCXI chassis. Modules currently supported include the SCXI-1124/116*X*/119*X*. The SCXI-1349 cable assembly can connect these modules to the NI 671*X*/673*X*.

Note The NI 671*X*/6733 for PXI cannot be used to control the SCXI portion of the PXI-1010/1011 chassis through the PXI backplane.

How can I approximate the frequency resolution of the analog output on the NI 671*X*/673*X*?

The analog frequency (f_a) you can generate is determined by the update clock frequency (f_u) and the number of samples per cycle (S_c) that you must choose, as Equation B-1 shows:

$$f_a = \frac{f_u}{S_c} \quad \text{(B-1)}$$

The onboard 20 MHz clock that generates f_u can only be divided by an integer. For example, to generate a clean sine wave at 2 kHz, you need 50 samples per cycle. According to Equation B-2, f_u is 100 kHz:

$$2 \text{ kHz} = \frac{f_u}{50} \quad \text{(B-2)}$$

For f_u to equal 100 kHz, the onboard clock must be divided by 200, as the following equality shows:

$$\frac{20 \text{ MHz}}{200} = 100 \text{ kHz}$$

The next available update clock you can generate occurs using a divisor of 199 or 201. If you choose 201, f_u equals 99.5 kHz, as the following equality shows:

$$\frac{20\ \text{MHz}}{201} = 99.50\ \text{kHz}$$

In this case, f_a equals 1.99 kHz, according to Equation B-3:

$$f_a = \frac{99.50\ \text{kHz}}{50} = 1.99\ \text{kHz} \quad \text{(B-3)}$$

The smallest frequency change that you can generate in this case is approximately 10 Hz. Another limiting factor could be the code width of the NI 671*X*/673*X*, but most users do not want that many samples to represent a cycle, so code width rarely becomes a factor.

Installing and Configuring the 671*X*/673*X* Device

How do you set the base address for the NI 671*X*/673*X* device?

The base address of the NI 671*X*/673*X* is automatically assigned through the bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring my NI 671*X*/673*X*?

The NI 671*X*/673*X* is jumperless and switchless.

Which NI document should I read first to get started using DAQ software?

The *DAQ Quick Start Guide* or application software release notes documentation are good places to start.

Analog Output

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When the DAC switches from one voltage to another, it produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can use a lowpass deglitching filter to remove some of these glitches, depending on the

frequency and nature of the output signal. In addition, if you are using this output as a source to a system that has low bandwidth characteristics, the glitches are ignored by the system.

Timing and Digital I/O

What types of triggering can be hardware-implemented on the NI 671*X*/673*X*?

Hardware digital triggering is supported on the NI 671*X*/673*X*.

What functionality does the DAQ-STC offer?

The DAQ-STC offers possible PFI lines, selectable logic level, and frequency shift keying. The DAQ-STC also supports buffered operations, such as direct up/down control, single pulse or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

I'm using one of the general-purpose counter/timers on the NI 671*X*/673*X*, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines are high-impedance.

What are the PFIs and how do I configure these lines?

PFIs are programmable function inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AO Clock Config, AO Trigger, Gate Config, and Counter Set Attribute advanced-level VIs to indicate which function the connected signal serves. Use the Route Signal VI to enable the PFI lines to output internal signals.

Caution If you enable a PFI line for output, do *not* connect any external signal source to it; if you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high-impedance by the hardware. This setting means that the device circuitry is not actively driving the output either high or low; however, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-3, *I/O Signal Summary for the NI 671X/673X*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) is in the high-impedance state after power on, and Table 4-3, *I/O Signal Summary for the NI 671X/673X*, shows that there is a 50 kΩ pull-up resistor. This pull-up resistor sets the DIO(0) pin to a logic high when the output is in a high-impedance state.

C

Technical Support and Professional Services

Visit the following sections of the NI Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
- **Training**—Visit ni.com/custed for self-paced tutorials, videos, and interactive CDs. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, NI Alliance Program members can help. To learn more, call your local NI office or visit ni.com/alliance.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Prefix	Meanings	Value
p-	pico	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}
t-	tera-	10^{12}

Numbers/Symbols

°	degrees
>	greater than
≥	greater than or equal to
<	less than
≤	less than or equal to
/	per
%	percent
±	plus or minus
+	positive of, or plus
–	negative of, or minus
Ω	ohms

$\sqrt{\ }$	square root of
+5 V	+5 VDC source signal

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions

B

bipolar	a signal range that includes both positive and negative values (for example, –5 to +5 V)

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
cm	centimeter

CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
counter/timer	a circuit that counts external pulses or clock pulses (timing)
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAQ	data acquisition—a system that uses the computer to collect, receive, and generate electrical signals
DAQ-STC	data acquisition system timing controller—an application-specific integrated circuit (ASIC) for the system timing requirements of a general A/D and D/A system, such as a system containing the NI E Series devices
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DI	digital input
DIFF	differential mode
DIO	digital input/output
DIP	dual inline package

dithering	the addition of Gaussian noise to an analog input signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output
DoC	Declaration of Conformity
DOC	Department of Communications

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
ESD	electrostatic discharge
EXTSTROBE	external strobe signal

F

FIFO	first-in first-out memory buffer—FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be read or written. For example, an analog input FIFO stores the results of A/D conversions until the data can be read into system memory. Programming the DMA controller and servicing interrupts can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored in the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
FPGA	field-programmable gate array

FREQ_OUT	frequency output signal
ft	feet

G

GATE	gate signal
GPCTR	general-purpose counter signal
GPCTR0_GATE	general-purpose counter 0 gate signal
GPCTR0_OUT	general-purpose counter 0 output signal
GPCTR0_SOURCE	general-purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general-purpose counter 0 up down signal
GPCTR1_GATE	general-purpose counter 1 gate signal
GPCTR1_OUT	general-purpose counter 1 output signal
GPCTR1_SOURCE	general-purpose counter 1 clock source signal
GPCTR1_UP_DOWN	general-purpose counter 1 up down signal

H

h	hour
hex	hexadecimal
Hz	hertz

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
INL	integral nonlinearity—for an ADC, deviation of codes of the actual transfer function from a straight line

I_{OH}	current, output high
I_{OL}	current, output low
IRQ	interrupt request

K

kHz	kilohertz

L

LED	light emitting diode
LSB	least significant bit

M

m	meter
MB	megabytes of memory
MHz	megahertz
MIO	multifunction I/O
MITE	MXI Interface to Everything
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel
mV	millivolts

N

NC	normally closed, or not connected
NI-DAQ	NI driver software for DAQ hardware

noise	an undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.
pd	pull-down
PFI	Programmable Function Input
PFI3/GPCTR1_ SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general-purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI8/GPCTR0_ SOURCE	PFI8/general-purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general-purpose counter 0 gate

port	(1) a communications connection on a computer or a remote controller; (2) a digital port, consisting of four or eight lines of digital input and/or output
ppm	parts per million
pu	pull-up

R

RAM	random access memory
reglitch	to modify the glitches in a signal in order to make them less disruptive
rms	root mean square
RSE	referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.
RTD	resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI bus	Real-Time System Integration bus—the NI timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise timing synchronization between multiple devices
RTSI_OSC	RTSI Oscillator—RTSI bus master clock

S

s	seconds
S	samples
SCANCLK	scan clock signal
SCXI	Signal Conditioning eXtensions for Instrumentation—the NI product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy computer environment

SE	single-ended—a term used to describe an analog input that is measured with respect to a common ground
settling time	the amount of time required for a voltage to reach its final value within specified limits
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
SOURCE	source signal
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count—the ending value of a counter
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
t_{out}	output delay time
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage
thermocouple	a temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TRIG	trigger signal
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic

U

UI	update interval
UISOURCE	update interval counter clock signal
unipolar	a signal range that is always positive (for example, 0 to +10 V)
UPDATE	update signal

V

V	volts
VDC	volts direct current
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument; (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
V_{rms}	volts, root mean square

W

WFTRIG	waveform generation trigger signal

Index

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